## Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

***PCN Title :*** Qualification of subcontractor TSHT (China) as additional assembly plant for selected products of General Purpose Analog Division in SO8 package
***PCN Reference :*** AMS/22/13298

***Subject :*** Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

| | | |
|---|---|---|
| MC33172DT | TSV912AIDT | TSV992IDT |
| TL062IDT | TS522IDT | TSV632AIDT |
| TSH22IDT | TS942AIDT | MC1458IDT |
| MC33078D | TS512AIDT | MC1458DT |
| TL431AIDT | TS1872AIDT | TSV358IDT |
| TS512IDT | TL431ACDT | MC33172D |
| TSV992AIDT | TS972IDT | TS482IDT |
| TSV632IDT | TSV912IDT | TS462CDT |
| TL062ID | TS942IDT | TL062BCDT |
| TS932IDT | TS1872IDT | TSV358AIDT |
| TL431CDT | TL062ACDT | TS1852IDT |
| LMV358IDT | MC33078DT | TS862IDT |
| TL431IDT | | |

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**PRODUCT/PROCESS**
CHANGE NOTIFICATION

PCN AMS/22/13298

# Analog, MEMS & Sensors (AMS)

## Extension of assembly site usage for additional products in SO8 package for General Purpose Analog

Reference: W130-TSHSTSO8-1

**WHAT:**

SO8 line in TSHT is in use for selected general purpose products for 5 years in volume. ST is pleased to announce the introduction of additional products on this line.

Please find more information related to material change in the table here below

| Material | Current process | Modified process | Comment |
|---|---|---|---|
| Diffusion location | ST Singapore<br>UMC (Taiwan) | ST Singapore<br>UMC (Taiwan) | No change |
| Assembly location | ST Bouskoura | TSHT China | |
| Molding compound | Sumitomo G700KC | Hitachi CEL-9220 | |
| Die attach | Ablestick 8601-S25 | Henkel 8200T | |
| Leadframe | Copper | Copper | |
| Plating | Matte Sn | Matte Sn | |
| Wire | Copper 1mil | Copper Pd coated 1 mil | |

**WHY:**

The purpose of the extension to additional product of usage of SO8 TSHT line for above listed commercial products is to provide a better support to our customers by enhancing the manufacturing process for higher volume production.

**HOW:**

The qualification program consists mainly of comparative electrical characterization and reliability tests.

You will find here after the qualification test plan which summarizes the various test methods and conditions that ST uses for this qualification program.

**Marking and traceability:**

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.

There is -as well- no change in the packing process or in the standard delivery quantities.
Shipments may start earlier with the customer's written agreement.

Reference: W130-TSHSTSO8-1

# External Reliability Evaluation Report

*New assy plant TSHT*

| General Information | |
|---|---|
| **Product Line** | 0158, UM37,0922, 3702, V802, LMV358LIPT |
| **Product Description** | Low power dual op-amps with low input bias current, Dual op amp, Dual comparator, Dual op amp |
| **P/N** | LM358DT, STMPS2141MTR, TS922IPT, TS3702IPT, |
| **Product Group** | AMG |
| **Product division** | GPA&RF |
| **Package** | SO8, TSSOP8 |
| **Silicon Process technology** | Bipolar, BCD6, HF2CMOS, HC1PA, HF5CMOS |

| Locations | |
|---|---|
| **Wafer fab** | Ang Mo Kio 6", ST Catania |
| **Assembly plant** | TSHT (TianShui Huatian Technology) China |
| **Reliability Lab** | Grenoble |

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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# 1 APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description |
|---|---|
| **AEC-Q100** | Stress test qualification for automotive grade integrated circuits |
| **AEC-Q101** | Stress test qualification for automotive grade discrete semiconductors |
| **JESD47** | Stress-Test-Driven Qualification of Integrated Circuits |
| | |

# 2 GLOSSARY

| | |
|---|---|
| **DUT** | Device Under Test |
| **PCB** | Printed Circuit Board |
| **SS** | Sample Size |
| | |

# 3 RELIABILITY EVALUATION OVERVIEW

## 3.1 Objectives

The objective of this qualification is to qualify a plant TSHT, for SO8 package for general purpose analog products
The line under qualification will serve several part numbers.
The qualification plan is based on the similarity and based on the JESD47 specification.

## 3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Reliability agreement for qualification.

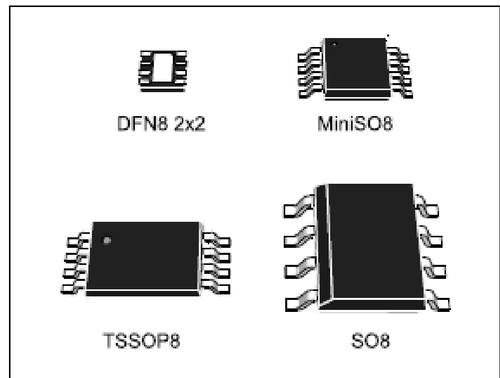
# 4 DEVICE CHARACTERISTICS

## 4.1 Device description

# LM158, LM258, LM358

## Low-power dual operational amplifiers

Datasheet - production data




### Features

- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current per channel essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 2 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rails
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to ($V_{CC}^+$ - 1.5 V)

### Related products

- See LM158W for enhanced ESD ratings

### Description

These circuits consist of two independent, high-gain, internally frequency-compensated op amps, specifically designed to operate from a single power supply over a wide range of voltages. The low-power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits, which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard 5 V, which is used in logic systems and will easily provide the required interface electronics with no additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.



This is information on a product in full production. www.st.com

# STMPS2141, STMPS2151, STMPS2161, STMPS2171

## Enhanced single channel power switches

Datasheet − production data

## Features

- 90 mΩ high-side MOSFET switch
- 500/1000 mA continuous current
- Thermal and short-circuit protection with overcurrent logic output
- Operating range from 2.7 to 5.5 V
- CMOS and TTL compatible enable input
- Undervoltage lockout (UVLO)
- 12 µA maximum standby supply current
- Ambient temperature range, -40 to 85 °C
- 8 kV ESD protection
- Reverse current protection
- Fault blanking
- UL recognized components (UL file number: E354278)

## Description

The STMPS2141, STMPS2151, STMPS2161, STMPS2171 power distribution switches are intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. These devices incorporate 90 mΩ N-channel MOSFET high-side power switches for power distribution. These switches are controlled by a logic enable input.

When the output load exceeds the current limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant current mode. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts the switch off to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until a valid input voltage is present.

Table 1. Device summary

| Order codes | | | Rated continuous output current (mA) | Enable |
|---|---|---|---|---|
| SO-8 | SOT23-5L | MSOP8(1) | | |
| STMPS2141MTR | STMPS2141STR | STMPS2141TTR | 500 | Active low |
| STMPS2151MTR | STMPS2151STR | STMPS2151TTR | 500 | Active high |
| STMPS2161MTR | STMPS2161STR | STMPS2161TTR | 1000 | Active low |
| STMPS2171MTR | STMPS2171STR | STMPS2171TTR | 1000 | Active high |

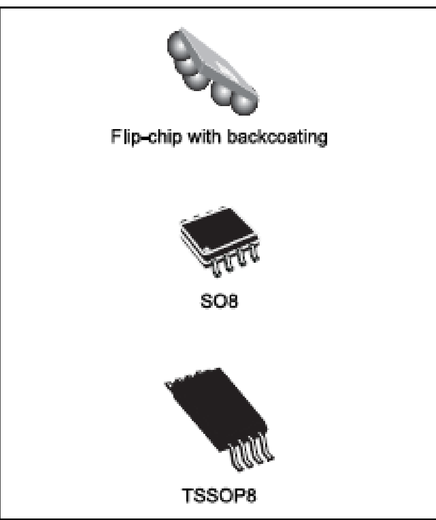
1. MSOP8 package is also known as "TSSOP8".

Reference: W130-TSHSTSO8-1

# TS922, TS922A

## Rail-to-rail, high output current, dual operational amplifier

Datasheet - production data




## Features

- Rail-to-rail input and output
- Low noise: 9 nV/√Hz
- Low distortion
- High output current: 80 mA (able to drive 32 Ω loads)
- High-speed: 4 MHz, 1 V/μs
- Operating from 2.7 to 12 V
- Low input offset voltage: 900 μV max. (TS922A)
- ESD internal protection: 2 kV
- Latch-up immunity
- Macromodel included in this specification
- Dual version available in Flip-chip package

## Applications

- Headphone and servo amplifiers
- Sound cards, multimedia systems
- Line drivers, actuator drivers
- Mobile phones and portable equipment
- Instrumentation with low noise as key factor
- Piezoelectric speaker drivers

## Description

TS922 and TS922A devices are rail-to-rail dual BiCMOS operational amplifiers optimized and fully specified for 3 V and 5 V operation. These devices have high output currents which allow low-load impedances to be driven.

Very low noise, low distortion, low offset, and a high output current capability make these devices an excellent choice for high quality, low voltage, or battery operated audio systems.

The devices are stable for capacitive loads up to 500 pF.

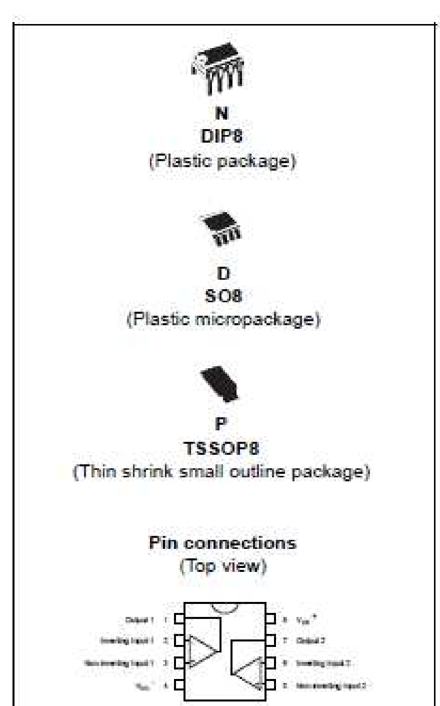
Reference: W130-TSHSTSO8-1

# TS3702

## Micropower dual CMOS voltage comparators

### Features

- Push-pull CMOS output (no external pull-up resistor required)
- Extremely low supply current: 9µA typ / comparator
- Wide single supply range: 2.7V to 16V or dual supplies (±1.35V to ±8V)
- Extremely low input bias current: 1pA typ
- Extremely low input offset currents: 1pA typ
- Input common-mode voltage range includes GND
- High input impedance: $10^{12}\Omega$ typ
- Fast response time: 2µs typ for 5mV overdrive
- Pin-to-pin and functionally compatible with bipolar LM393




### Description

The TS3702 is a micropower CMOS dual voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM393). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.

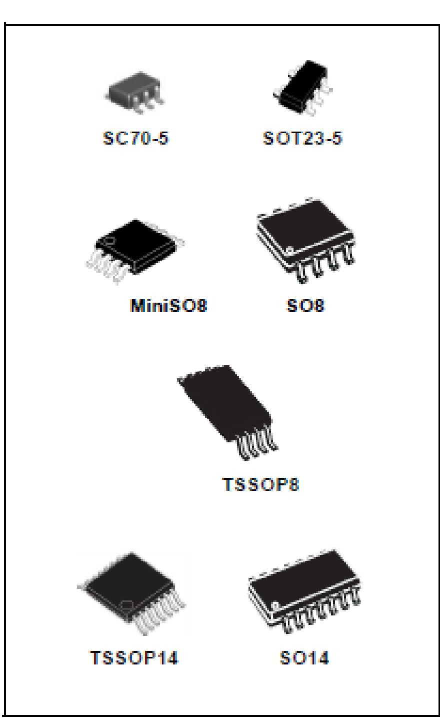
Thus response times remain similar to the LM393.

Reference: W130-TSHSTSO8-1

# LMV321L, LMV358L, LMV324L

## Low-power, general-purpose operational amplifiers

**Datasheet - production data**




## Features

- Low-power consumption: 250 µA max at 5 V
- Low offset voltage: 7 mV max at 25 °C
- Industrial temperature range: -40 °C to +125 °C
- Low supply voltage: 2.7 V - 5.5 V
- Gain bandwidth product: 1.3 MHz
- Tiny packages

## Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

## Description

The LMV321L, LMV358L, and LMV324L are single, dual, and quad operational amplifiers with rail-to-rail output capabilities. They are specifically designed to operate at low voltages (2.7 V to 5 V) with enhanced performances compared to the industry standard LM3xx series.

The LMV321L, LMV358L, and LMV324L are offered in tiny packages, allowing the devices to be used in small portable electronic applications and to be placed closer to the actual signal.

The LMV321L, LMV358L, and LMV324L are complete cost-effective solutions for application designs where cost is of primary importance.

# Construction note

| | New Plant Qualification | | | | |
|---|---|---|---|---|---|
| | **P/N LM358DT** | **P/N: STMPS2141MTR** | **P/N TS922IPT** | **P/N TS3702IPT** | **P/N LMV358LIPT** |
| **Wafer/Die fab. information** | | | | | |
| Wafer fab manufacturing location | ST Singapore | ST Catania | ST Singapore | ST Singapore | UMC Taiwan |
| Technology | PRO450S-C | BCD6 | HF2CMOS | HC1PA | HF5CMOS |
| Process family | Bipolar | BCD6 | HF2CMOS | HC1PA | HF5CMOS |
| Die finishing back side | Raw Silicon | Raw Silicon | Raw Silicon | Lapped silicon | Lapped silicon |
| Die size | 1070 x 1010 µm² | 2198x0698µm² | 1720x1190µm² | 1366x1136µm² | 1062x802µm² |
| Passivation type | SiN (nitride) | TEOS/SiN/Polyimide | PVAPOX+Nitride | PVAPOX+Nitride | USG-PSG-SiON-PIX |
| **Wafer Testing (EWS) information** | | | | | |
| Electrical testing manufacturing location | ST SINGAPORE | ST SINGAPORE | ST SINGAPORE | ST SINGAPORE | ST SINGAPORE |
| **Assembly information** | | | | | |
| Assembly site | TSHT | TSHT | TSHT | TSHT | TSHT |
| Package description | SO8 | SO8 | TSSOP8 | TSSOP8 | TSSOP8 |
| Molding compound | Hitachi CEL-9220 | Hitachi CEL-9220 | Hitachi CEL-9220 | Hitachi CEL-9220 | Hitachi CEL-9220 |
| Frame material | Copper | Copper | Copper | Copper | Copper |
| Die attach process | Glue | Glue | Glue | Glue | Glue |
| Die attach material | Ablestik - 8200T- | Ablestik - 8200T | Ablestik - 8200T | Ablestik - 8200T | Ablestik - 8200T |
| Wire bonding process | Wire | Wire | Wire | Wire | Wire |
| Wires bonding materials/diameters | 1.0mil PdCu | 1.3mil Gold | 1.0mil PdCu | 1.0mil PdCu | 1.0mil PdCu |
| Lead finishing process | Copper | Copper | Copper | Copper | Copper |
| Lead finishing/bump solder material | Sn | Sn | Sn | Sn | Sn |
| **Final testing information** | | | | | |
| Testing location | TSHT | TSHT | TSHT | TSHT | TSHT |

# 5 TESTS RESULTS SUMMARY

## 5.1 Test vehicle

| Lot # | Process/ Package | Product Line | Comments |
|---|---|---|---|
| 1 | SO8/Bipolar | 0158 | |
| 2 | SO8/Bipolar | 0158 | |
| 3 | SO8/Bipolar | 0158 | |
| 4 | SO8/BCD6 | UM37 | |
| 5 | SO8/BCD6 | UM37 | |
| 6 | SO8/BCD6 | UM37 | |
| 7 | TSSOP8/HF2CMOS | 0922 | |
| 8 | TSSOP8/HC1PA | 3702 | |
| 9 | TSSOP8/HF5CMOS | V802 | |

Detailed results in below chapter will refer to P/N and Lot #.

## 5.2 Test plan and results summary

**P/N LM358DT**

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS Lot 1 | Failure/SS Lot 2 | Failure/SS Lot 3 | Note |
|---|---|---|---|---|---|---|---|---|---|
| **Die Oriented Tests** | | | | | | | | | |
| HTOL | N | JESD22 A-108 | Tj = 125°C, BIAS | 80 | 168 H | **0/80** | **0/80** | **0/80** | |
| | | | | | 500 H | **0/80** | **0/80** | **0/80** | |
| | | | | | 1000 H | **0/80** | **0/80** | **0/80** | |
| HTSL | N | JESD22 A-103 | Ta = 150°C | | 168 H | **0/77** | **0/77** | | |
| | | | | | 500 H | | | | |
| | | | | | 1000 H | **0/77** | **0/77** | | |
| ELFR | N | AEC Q100 - 008 | | 400 | 48H | **0/400** | **0/401** | **0/396** | |
| **Package Oriented Tests** | | | | | | | | | |
| PC | | JESD22 A-113 | Drying 24 H @ 125°C<br>Store 192 H @ Ta=30°C Rh=60%<br>Over Reflow @ Tpeak=260°C 3 times | | Final | **PASS** | **PASS** | **PASS** | |
| uHAST | Y | JESD22 A-118 | T°=130°C; Pressure=2.3 atm; HR=85% | | 96 H | **0/80** | **0/80** | | |
| THS | Y | JESD22 A-110 | Ta = 85°C, RH = 85%, | | 168 H | **0/80** | | | |
| | | | | | 1000 H | **0/80** | | | |
| TC | Y | JESD22 A-104 | Ta = -65°C to 150°C | | 100 cy | **0/77** | **0/77** | | |
| | | | | | 1000 cy | **0/77** | **0/77** | | |
| THB | Y | JESD22 A-101 | Ta = 85°C, RH = 85%, BIAS | | 168 H | **0/77** | **0/77** | **0/77** | |
| | | | | | 500 H | **0/77** | **0/77** | **0/77** | |
| | | | | | 1000 H | **0/77** | **0/77** | **0/77** | |
| **Other Tests** | | | | | | | | | |
| ESD | N | AEC Q101-001, 002 and 005 | CDM | 3 | 1.5kV | **PASS** | | | |

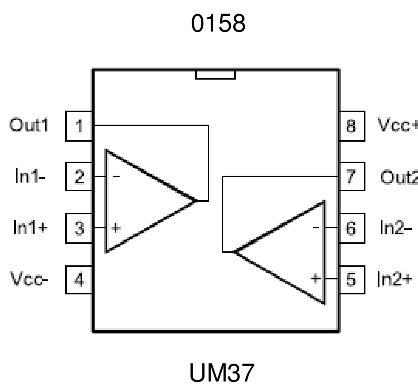
| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Lot 4 UM37 | Lot 5 UM37 | Lot 6 UM37 | Lot 7 0922 | Lot 8 3702 | Lot9 V802 | | |
| HTOL | N | JESD22 A-108 | Ta=125°C, BIAS | | 168 H | | | | 0/77 | 0/77 | 0/77 | | |
| | | | | | 500 H | | | | 0/77 | 0/77 | 0/77 | | |
| | | | | | 1000 H | | | | 0/77 | 0/77 | 0/77 | | |
| | | | | | | | | | | | | | |
| HTSL | N | JESD22 A-103 | Ta = 150°C | | 168 H | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | | |
| | | | | | 500 H | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | | |
| | | | | | 1000 H | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | | |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| PC | | JESD22 A-113 | Drying 24 H @ 125°C<br>Store 168 H @ Ta=85°C<br>Rh=85%<br>Over Reflow @ Tpeak=260°C 3 times | | Final | PASS | PASS | PASS | PASS | PASS | PASS | | |
| UHAST | Y | JESD22 A-102 | 85%RH / Ta=130°C | | 96 H | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | | |
| TC | Y | JESD22 A-104 | Ta = -55°C to 150°C | | 100 cy | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | | |
| | | | | | 200 cy | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | | |
| | | | | | 500 cy | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | 0/77 | | |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| THB | Y | JESD22 A-101 | Ta = 85°C, RH = 85%, BIAS | | 168 H | | | | 0/77 | 0/77 | 0/77 | | |
| | | | | | 500 H | | | | 0/77 | 0/77 | 0/77 | | |
| | | | | | 1000 H | | | | 0/77 | 0/77 | 0/77 | | |
| | | | | | | | | | | | | | |

# 6 ANNEXES

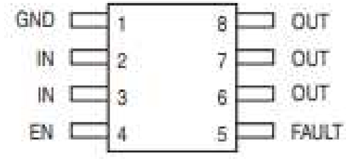
## 6.1 Device details

### 6.1.1 Pin connection

0158




UM37



### 6.1.2 Package outline/Mechanical data

PACKAGE OUTLINE ASSEMBLY

TITLE: POA SO 8L

PLANT CODE: 999L
PACKAGE CODE: O7
PACKAGE WEIGHT: 0,0765 g/unit typ
JEDEC REFERENCE NUMBER: JEDEC MS-012-AA

Option C

PACKAGE DIMENSIONS

| DATABOOK | | | | |
|---|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. | NOTE |
| A | - | - | 1.75 | |
| A1 | 0.10 | - | 0.225 | |
| A2 | 1.30 | 1.40 | 1.50 | |
| A3 | 0.60 | 0.65 | 0.70 | |
| b | 0.39 | - | 0.47 | |
| b1 | 0.38 | 0.41 | 0.44 | |
| c | 0.20 | - | 0.24 | |
| c1 | 0.19 | 0.20 | 0.21 | |
| D | 4.80 | 4.90 | 5.00 | |
| E | 5.80 | 6.00 | 6.20 | |
| E1 | 3.80 | 3.90 | 4.00 | |
| e | | 1.27BSC | | |
| L1 | | 1.05REF | | |
| h | 0.25 | - | 0.50 | |
| L | 0.50 | - | 0.80 | |
| Θ | 0 | - | 8° | |

NOTES:

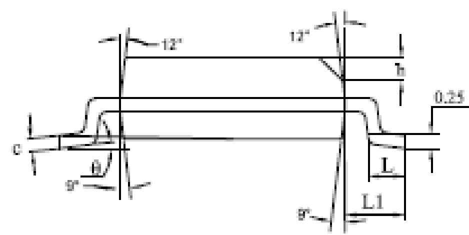
1. Controlling Dimension: MILLIMETER
2. Package outline exclusive of any mold flashes dimensions and metal burrs
3. Max resin gate protrusion : 0.20mm

Reference: W130-TSHSTSO8-1

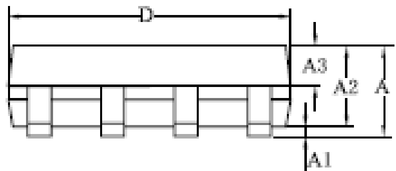
# PLANT CODE: 999L

## SO 8L

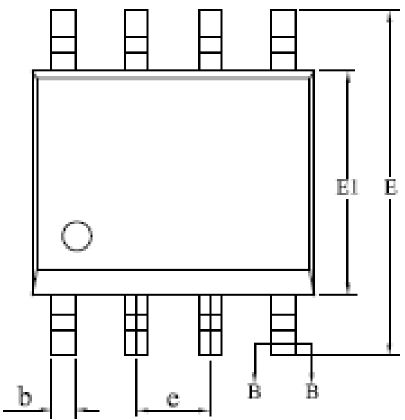
### SIDE VIEW




### SIDE VIEW

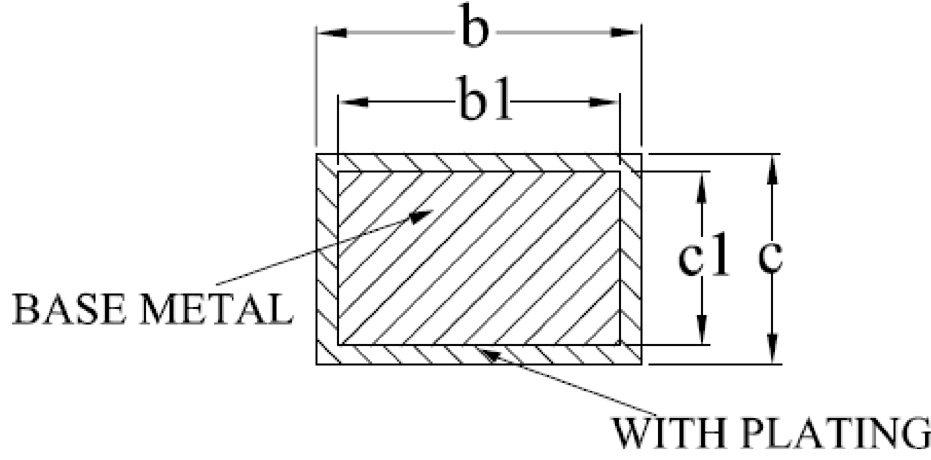



### TOP VIEW



# PLANT CODE: 999L

## SO 8L



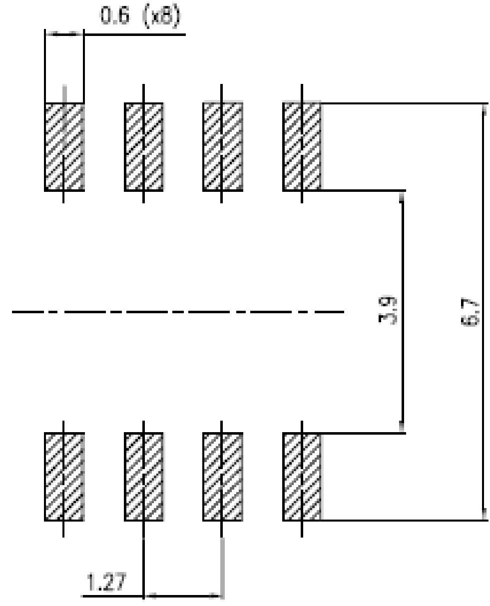

SECTION B-B

Reference: W130-TSHSTSO8-1

| | FIGURE : 2 | DOC. NUMBER : 0016023 |
|---|---|---|

TITLE : PLASTIC SMALL OUTLINE PACKAGE 8L

# RECOMMENDED FOOTPRINT




MATERIAL

NATIVE SCALE

PROJECTION

DIM are in mm – Unspecified tolerance

| Precision rate | 0 mm 6 mm | 6,01 mm 30 mm | 30,01mm 120 mm | 120,01mm 315 mm | over 315 mm | Angular |
|---|---|---|---|---|---|---|
| Coarse | ±0.2 | ±0.5 | ±0.8 | ±1.2 | ±2 | ±1° |
| Medium | ±0.1 | ±0.2 | ±0.3 | ±0.5 | ±0.8 | ±0°30' |
| Fine | ±0.05 | ±0.1 | ±0.15 | ±0.2 | ±0.3 | ±0°20' |

## 6.2 Tests Description

| Test name | Description | Purpose |
|---|---|---|
| **Die Oriented** | | |
| **HTOL**<br>Higt Temperature Operating Life<br><br>**HTB**<br>High Temperature Bias | The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition. | To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way.<br>The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults. |
| **HTSL**<br>High Temperature Storage Life | The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature. | To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding. |
| **ELFR**<br>Early Life Failure Rate | The device is stressed in biased conditions at the max junction temperature. | To evaluate the defects inducing failure in early life. |
| **Package Oriented** | | |
| **PC**<br>Preconditioning | The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption. | As stand-alone test: to investigate the moisture sensitivity level.<br>As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance.<br>The typical failure modes are "pop corn" effect and delamination. |
| **AC**<br>Auto Clave (Pressure Pot) | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature. | To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. |
| **TC**<br>Temperature Cycling | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere. | To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation. |
| **THB**<br>Temperature Humidity Bias | The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity. | To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence. |
| **Other** | | |
| **ESD**<br>Electro Static Discharge | The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models.<br>**CBM**: Charged Device Model<br>**HBM**: Human Body Model<br>**MM**: Machine Model | To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge. |

Annex 1: Other results

Wire pull test

| Value in gram (min limit 4g) | | | | | | |
|---|---|---|---|---|---|---|
| | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Unit 6 |
| | 23.67 | 23.97 | 22.2 | 21.1 | 22.17 | 20.99 |
| | 24.06 | 23.24 | 23.14 | 20.26 | 19.5 | 24.18 |
| | 19.33 | 24.01 | 21.18 | 23 | 25.42 | 19.36 |
| | 19.58 | 22.17 | 20.99 | 21.15 | 24.64 | 22.17 |
| | 20.16 | 20.35 | 24.87 | 22.87 | 24.2 | 20.5 |
| | 20.48 | 20.69 | 22.96 | 21.55 | 22.5 | 25.97 |
| | 20.77 | 21.29 | 21.34 | 21.51 | 21.3 | 24.64 |
| | 21.65 | 21.79 | 20.85 | 23.26 | 23.31 | 24.2 |
| Min(g) | 19.33 | | | | | |
| Max(g) | 25.97 | | | | | |
| average(g) | 22.09 | | | | | |
| cpl | 3.56 | | | | | |

Wire shear test

| Value in gram (min limit 18g) | | | | | | |
|---|---|---|---|---|---|---|
| | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Unit 6 |
| | 46.89 | 49.58 | 48.33 | 49.26 | 46.21 | 46.88 |
| | 48.15 | 46.33 | 46.27 | 47.55 | 48.71 | 49.54 |
| | 45.25 | 49.88 | 16.86 | 45.65 | 49.55 | 49.67 |
| | 48.22 | 48.37 | 48.17 | 48.14 | 46.35 | 49.18 |
| | 47.36 | 48.16 | 46.88 | 49.33 | 45.33 | 49.24 |
| | 48.31 | 48.87 | 47.33 | 48.98 | 49.36 | 48.98 |
| | 49.16 | 49.33 | 45.33 | 50.17 | 48.71 | 48.36 |
| | 48.24 | 47.24 | 46.24 | 48.98 | 49.36 | 48.78 |
| Min (g) | 16.86 | | | | | |
| Max (g) | 50.17 | | | | | |
| Average (g) | 46.67 | | | | | |
| cpl | 2.05 | | | | | |

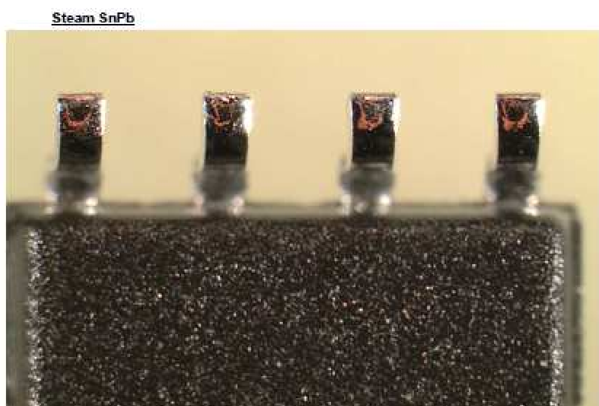
Conclusion: in line with ST specification

Solderability
Coverage minimum 95% after dipping

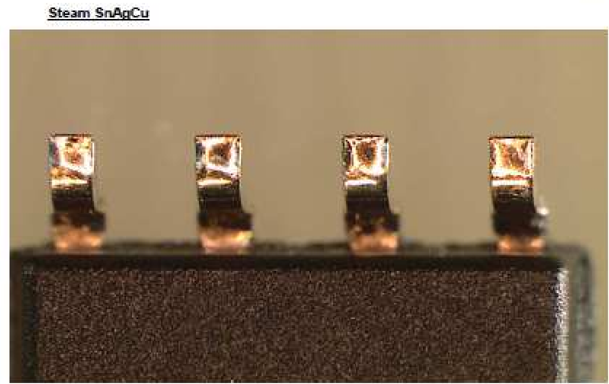
| PACKAGE | SOLDER BATH | SOLDER BATH TEMP. | SOLDER DIPPING TIME | AGING | SAMPLING | REJECT |
|---|---|---|---|---|---|---|
| **Lead finishing Sn Preplated** | SnPb | 220°C | 10s | 8h steam @85°C/85HR | 10 | 0 |
| | | | 10s | 16hrs dry air @150°C | 10 | 0 |
| | SnAgCu | 245°C | 10s | 8h steam @85°C/85HR | 10 | 0 |
| | | | 10s | 16hrs dry air @150°C | 10 | 0 |

**Dry air SnAgCu**

**Steam SnPb**



**Steam SnAgCu**



**Dry air SnPb**

Conclusion: in line with ST specification.

Electrical distribution compare to part produce in ST Bouskoura

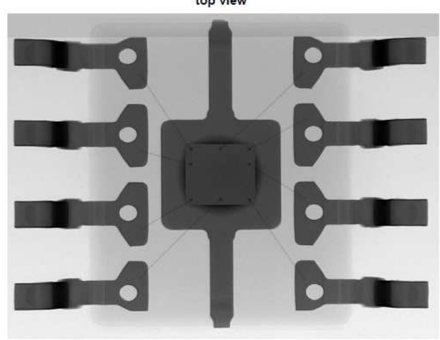
| | Units | MEAN | | | CPK | |
|---|---|---|---|---|---|---|
| | | TSHT | BSK | Mean Drift | TSHT | Comments |
| P106_*0 | mA | 0.45 | 0.46 | -0.01 | 50.38 | OK |
| P101_A0 | mV | 0.26 | 0.49 | -0.23 | 3.03 | OK |
| P101_B0 | mV | 0.98 | 1.26 | -0.27 | 3.07 | OK |
| P117_A0 | V | 28.52 | 28.53 | -0.01 | 8.11 | OK |
| P117_B0 | V | 28.53 | 28.52 | 0.01 | 8.55 | OK |
| P117_A0 | V | 0.00 | 0.00 | 0.00 | 10.11 | OK |
| P117_B0 | V | 0.00 | 0.00 | 0.00 | 9.14 | OK |
| P106_*1 | mA | 0.56 | 0.62 | -0.05 | 30.83 | OK |
| P101_A1 | mV | 0.25 | 0.46 | -0.21 | 2.82 | OK |
| P101_B1 | mV | 1.00 | 1.23 | -0.23 | 2.38 | OK |
| P106_*3 | mA | 0.47 | 0.50 | -0.03 | 13.11 | OK |
| P101_A3 | mV | 0.24 | 0.47 | -0.23 | 2.86 | OK |
| P101_B3 | mV | 0.98 | 1.23 | -0.25 | 2.43 | OK |
| P101_A2 | mV | -0.03 | 0.23 | -0.26 | 2.97 | OK |
| P101_B2 | mV | 0.68 | 0.99 | -0.31 | 2.66 | OK |
| P105_A1 | dB | 128.55 | 129.38 | -0.83 | n/a . | OK |
| P105_B1 | dB | 119.44 | 133.49 | -14.05 | n/a . | OK |
| P109_A1 | dB | 100.65 | 102.89 | -2.24 | n/a . | OK |
| P109_B1 | dB | 99.57 | 102.83 | -3.26 | n/a . | OK |
| P104_A1 | V/mV | 302.14 | 253.98 | 48.15 | n/a . | OK |
| P104_B1 | V/mV | 318.47 | 259.78 | 58.69 | n/a . | OK |
| P115_*1 | n/a | 1.00 | 1.00 | 0.00 | n/a . | OK |
| P150_*1 | V | 5.00 | 5.00 | 0.00 | 3024.28 | OK |
| P117_A3 | mV | 0.00 | 0.00 | 0.00 | 8.43 | OK |
| P117_B3 | mV | 0.00 | 0.00 | 0.00 | 8.29 | OK |
| P117_A1 | V | 28.20 | 28.45 | -0.24 | 70.80 | OK |
| P117_B1 | V | 28.21 | 28.44 | -0.23 | 69.45 | OK |
| P117_A5 | V | 8.52 | 8.53 | -0.01 | 14.79 | OK |
| P117_B5 | V | 8.53 | 8.53 | -0.01 | 14.46 | OK |
| P117_A3 | V | 3.62 | 3.59 | 0.03 | 8.21 | OK |
| P117_B3 | V | 3.62 | 3.59 | 0.03 | 8.13 | OK |
| P101_A31 | mV | 0.00 | 0.00 | 0.00 | 3.19 | OK |
| P101_B31 | mV | 0.00 | 0.00 | 0.00 | 3.28 | OK |
| P102_A1 | nA | -1.85 | 0.00 | -1.85 | n/a . | OK |
| P102_B1 | nA | -3.92 | 0.00 | -3.92 | n/a . | OK |
| P103_A1 | µA | -0.0395 | -0.0311 | -0.0084 | n/a . | OK |
| P103_B1 | µA | -0.0403 | -0.0324 | -0.0079 | n/a . | OK |
| P103_A1 | µA | -0.0377 | -0.0306 | -0.0071 | n/a . | OK |
| P103_B1 | µA | -0.0364 | -0.0298 | -0.0066 | n/a . | OK |
| P137_A2 | mA | 0.0180729 | 0.0183346 | -0.0002617 | 20.07 | OK |
| P137_B2 | mA | 0.0182641 | 0.0184874 | -0.0002233 | 18.19 | OK |
| P137_A1 | mA | -0.03 | -0.03 | 0.00 | 18.23 | OK |
| P137_B1 | mA | -0.03 | -0.03 | 0.00 | 20.08 | OK |
| P137_A21 | mA | 0.08 | 0.00 | 0.08 | 13.39 | OK |
| P137_B21 | mA | 0.08 | 0.00 | 0.08 | 10.34 | OK |
| P121_A1 | MHz | 1.19 | 1.27 | -0.08 | 13.47 | OK |
| P121_B1 | MHz | 1.22 | 1.27 | -0.05 | 13.07 | OK |
| P113_A2 | V/uS | 0.84 | 0.82 | 0.02 | 20.08 | OK |
| P113_B2 | V/uS | 0.85 | 0.86 | -0.01 | 19.50 | OK |
| P113_A2 | V/uS | 0.73 | 0.71 | 0.02 | 15.39 | OK |
| P113_B2 | V/uS | 0.73 | 0.74 | -0.01 | 20.00 | OK |

**No CPK calculation done on the Iib, AVD, CMR, SVR as they are not gaussian**

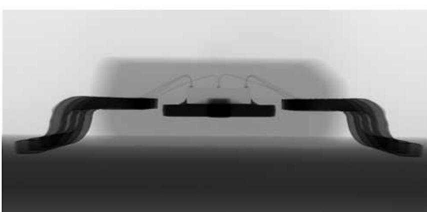
Reference: W130-TSHSTSO8-1

Xray pictures

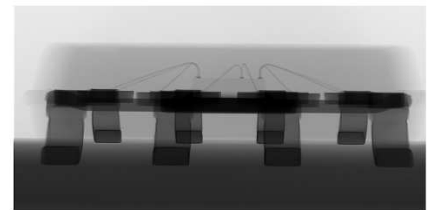
top view



side 1 view 45°



side 2 view 45°



Process flow chart:

| 序号 NO. | 工艺流程 PROCESS FLOW | 工艺步骤 PROCESS STEP |
|---|---|---|
| | | 晶圆&芯片 Wafer & Chip |
| | | 反馈客户 Feedback Customer |
| 1 | Pass / Fail | 晶圆进料检验 Wafer IQC |
| 2 | BG TAPE | 晶圆正面贴膜(可选) BG Tape(Option) |
| 3 | Back Grinding | 减薄 Back Grinding |
| 4 | Wafer Mounting | 贴片 Wafer Mounting |
| 5 | WFT_BK | 贴片预烘烤Wafer Mounted Tape rebake |
| 6 | Wafer Sawing | 划片 Wafer Sawing |
| | | 引线框架 Lead frame |
| | | 贴片材料 Die Attach Material |
| 7 | Die Bonding | 上芯 Die Bonding |
| 8 | DA Curing | 上芯烘烤 DA Curing |

| 序号 NO. | 工艺流程 PROCESS FLOW | 工艺步骤 PROCESS STEP |
|---|---|---|
| 9 | Plasma before W/B | 压焊前清洗 Plasma before Wire bond |
| | | 焊线 Bonding Wire |
| 10 | Wire bonding | 压焊 Wire Bonding |
| 11 | | 品管检验 QC Gate |
| | | 塑封料 Mold Compound |
| 12 | Molding | 塑封 Molding |
| 13 | PMC | 后固化 Post Mold Curing |
| | | 锡球 Pin Sn |
| 14 | Plating | 电镀 Plating |
| 15 | Cure after Plating | 电镀后烘烤 Cure after Plating |
| 16 | Laser Marking | 激光打印 Laser Marking |

| 序号 NO. | 工艺流程 PROCESS FLOW | 工艺步骤 PROCESS STEP |
|---|---|---|
| 17 | Trim/Form/ Singulation | 切筋/成形/分离 Trim/Form/Singulation |
| 18 | | 品管检验 QC Gate |
| 19 | FT | 测试（可选） Testing(Option) |
| 20 | | EQC品管检验（可选） EQC Gate (Option) |
| 21 | | VI 品管检验（可选） Visual Inspection Gate(Option) |
| 22 | Packing | 包装 Packing |
| 23 | | 品管检验 Outgoing quality control |
| 24 | Shipping | 发货 Shipping |

Reference: W816-TSHSTSO8-2

# External Reliability Evaluation Report

*New assembly plant TSHT with 70x70LF*

| General Information | |
|---|---|
| **Product Line** | 0158, 0922, 0082, LA05, KS33 |
| **Product Description** | Low power dual op-amps with low input bias current, Rail-to-rail, high output current, dual operational amplifier, LDO |
| **P/N** | LM358DT, TS922IDT, L78L05, LD1117 |
| **Product Group** | AMS |
| **Product division** | GPA&RF |
| **Package** | SO8 |
| **Silicon Process technology** | Bipolar, HF2CMOS, HBIP40 |

| Locations | |
|---|---|
| **Wafer fab** | Ang Mo Kio 6” |
| **Assembly plant** | TSHT (TianShui Huatian Technology) China |
| **Reliability Lab** | Grenoble |

## DOCUMENT INFORMATION

| Version | Date | Pages | Comment |
|---|---|---|---|
| 1.0 | 6-oct-2017 | 12 | First issue |
| 2.0 | 19-Apr-2018 | 12 | Plan for large LF Pad |
| | | | |

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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# 1 APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description |
|---|---|
| **AEC-Q100** | Stress test qualification for automotive grade integrated circuits |
| **AEC-Q101** | Stress test qualification for automotive grade discrete semiconductors |
| **JESD47** | Stress-Test-Driven Qualification of Integrated Circuits |
| | |

# 2 GLOSSARY

| | |
|---|---|
| **DUT** | Device Under Test |
| **PCB** | Printed Circuit Board |
| **SS** | Sample Size |
| | |

# 3 RELIABILITY EVALUATION OVERVIEW

## 3.1 Objectives

The objective of this evaluation is to qualify the subcontractor TSHT for the assembly of selected product in SO8 package.
The line under qualification will serve several part numbers.
The qualification plan is based on the similarity and based on the JESD47 specification.
Here below are the details of the change depending on the affected product.

From ST Bouskoura to TSHT (see annex for product list)

| Material | Current process | Modified process | Comment |
|---|---|---|---|
| Diffusion location | No change | | |
| Assembly location | ST Bouskoura | TSHT | |
| Molding compound | Sumitomo G700KC | Hitachi CEL-9220 | |
| Die attach | Ablestick 8601-S25 | Ablestik -Ablecoat 8200T | |
| Lead-frame | Copper | Copper | |
| Wire | Copper 1 mil | Copper 1 mil Pd coated | |
| Plating | Sn | Sn | |

From ST Shenzhen to TSHT (see annex for product list)

| Material | Current process | Modified process | Comment |
|---|---|---|---|
| Diffusion location | No change | | |
| Assembly location | ST Shenzhen | TSHT | |
| Molding compound | Sumitomo G700KC | Hitachi CEL-9220 | |
| Die attach | Ablestick 8601-S25 | Ablestik -Ablecoat 8200T | |
| Lead-frame | Copper | Copper | |
| Wire | Copper 1 mil | Copper 1 mil | |
| Plating | NiPdAgAu | Sn | |

## 3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Reliability agreement for qualification.

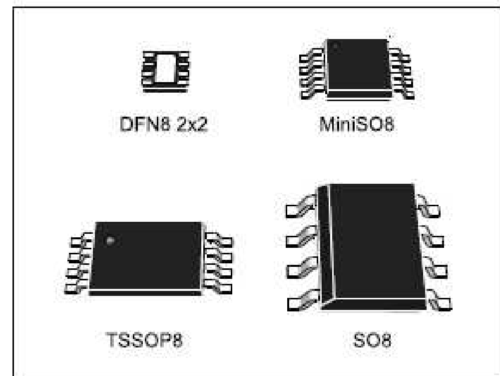
# 4 DEVICE CHARACTERISTICS

## 4.1 Device description

# LM158, LM258, LM358

Low-power dual operational amplifiers

Datasheet - production data




### Features

- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current per channel essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 2 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rails
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to ($V_{CC}^{+}$ - 1.5 V)

### Related products

- See LM158W for enhanced ESD ratings

### Description

These circuits consist of two independent, high-gain, internally frequency-compensated op amps, specifically designed to operate from a single power supply over a wide range of voltages. The low-power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits, which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard 5 V, which is used in logic systems and will easily provide the required interface electronics with no additional power supply.

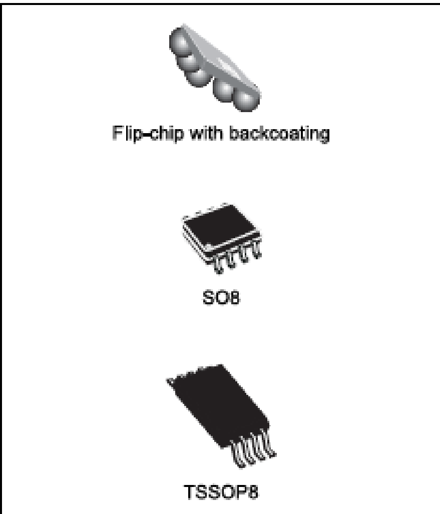
In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

Reference: W816-TSHSTSO8-2

# TS922, TS922A

## Rail-to-rail, high output current, dual operational amplifier

Datasheet - production data




## Features

- Rail-to-rail input and output
- Low noise: 9 nV/√Hz
- Low distortion
- High output current: 80 mA (able to drive 32 Ω loads)
- High-speed: 4 MHz, 1 V/μs
- Operating from 2.7 to 12 V
- Low input offset voltage: 900 μV max. (TS922A)
- ESD internal protection: 2 kV
- Latch-up immunity
- Macromodel included in this specification
- Dual version available in Flip-chip package

## Applications

- Headphone and servo amplifiers
- Sound cards, multimedia systems
- Line drivers, actuator drivers
- Mobile phones and portable equipment
- Instrumentation with low noise as key factor
- Piezoelectric speaker drivers

## Description

TS922 and TS922A devices are rail-to-rail dual BiCMOS operational amplifiers optimized and fully specified for 3 V and 5 V operation. These devices have high output currents which allow low-load impedances to be driven.

Very low noise, low distortion, low offset, and a high output current capability make these devices an excellent choice for high quality, low voltage, or battery operated audio systems.

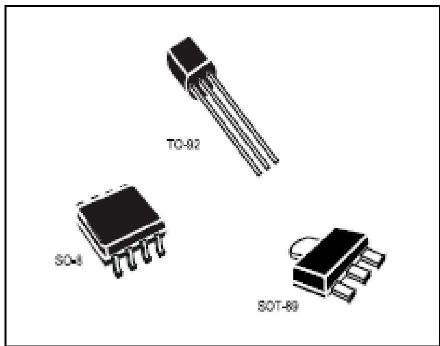
The devices are stable for capacitive loads up to 500 pF.

Reference: W816-TSHSTSO8-2

# L78L

## Positive voltage regulators

Datasheet - production data




## Features

- Output current up to 100 mA
- Output voltages of 3.3; 5; 6; 8; 9; 10; 12; 15; 18; 24 V thermal overload protection
- Short-circuit protection
- No external components are required
- Available in either ± 4% (A) or ± 8% (C) selection

## Description

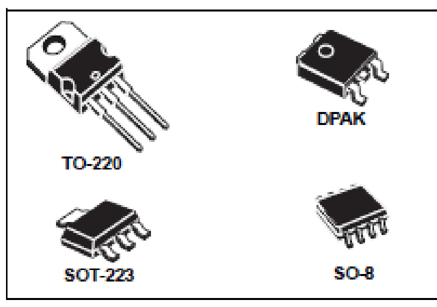
The L78L series of three-terminal positive regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heat-sink is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators. The L78L series used as Zener diode/resistor combination replacement, offers e improvement along with lower quiescent current and lower noise.

Reference: W816-TSHSTSO8-2

# LD1117

## Adjustable and fixed low drop positive voltage regulator

Datasheet - production data




## Features

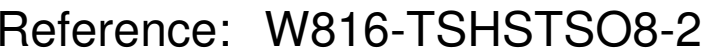
- Low dropout voltage (1 V typ.)
- 2.85 V device performances are suitable for SCSI-2 active termination
- Output current up to 800 mA
- Fixed output voltage of: 1.2 V, 1.8 V, 2.5 V, 3.3 V, 5.0 V
- Adjustable version availability ($V_{REF}$ = 1.25 V)
- Internal current and thermal limit
- Available in ± 1 % (at 25 °C) and 2 % in full temperature range
- Supply voltage rejection: 75 dB (typ.)

## Description

The LD1117 is a low drop voltage regulator able to provide up to 800 mA of output current, available even in adjustable version ($V_{REF}$ = 1.25 V). Concerning fixed versions, are offered the following output voltages: 1.2 V, 1.8 V, 2.5 V, 2.85 V, 3.3 V and 5.0 V. The device is supplied in: SOT-223, DPAK, SO-8 and TO-220. The SOT-223 and DPAK surface mount packages optimize the thermal characteristics even offering a relevant space saving effect. High efficiency is assured by NPN pass transistor. In fact in this case, unlike than PNP one, the quiescent current flows mostly into the load. Only a very common 10 µF minimum capacitor is needed for stability. On chip trimming allows the regulator to reach a very tight output voltage tolerance, within ± 1 % at 25 °C. The adjustable LD1117 is pin to pin compatible with the other standard. Adjustable voltage regulators maintaining the better performances in terms of drop and tolerance.

# 5 CONSTRUCTION NOTE

| | New Plant Qualification | | | |
|---|---|---|---|---|
| | **P/N LM358DT** | **PN/TS922IDT** | **P/N L78L05ABD13TR** | **P/N LD1117D33CTR** |
| **Wafer/Die fab. information** | | | | |
| Wafer fab manufacturing location | AM6F (Singapore) | | | |
| Technology | Bipolar | HF2CMOS | HBIP40 | Bipolar |
| Process family | Bipolar | BiCMOS2 | Bipolar | Bipolar |
| Die finishing back side | Raw Silicon | Raw Silicon | Lapped silicon | CrNiAg |
| Die size | 1070 x 1010 $\mu m^2$ | 1720x1190$\mu m^2$ | 766 x 706 $um^2$ | 1990 x 1860$um^2$ |
| Passivation type | SiN (nitride) | PVAPOX+Nitride | PVAPOX+Nitride | SiN (nitride) |
| **Assembly information** | | | | |
| Assembly site | SC-Tianshui Huatian-China (TSHT) | | | |
| Package description | SO8 | | | |
| Molding compound | Hitachi CEL-9220 | | | |
| Frame material | Copper 70x70 | Copper 90x90 | Copper 94x125 | Copper 94x125 |
| Die attach process | Glue | | | |
| Die attach material | Ablestik -Ablecoat 8200T- | | | |
| Wire bonding process | Wire | | | |
| Wires bonding materials/diameters | 1.0mil PdCu | | | |
| Lead finishing process | Copper | | | |
| Lead finishing/bump solder material | Sn | | | |
| **Final testing information** | | | | |
| Testing location | SC-Tianshui Huatian-China (TSHT) 999L | | | |



# 6 TESTS RESULTS SUMMARY

## 6.1 Test vehicle

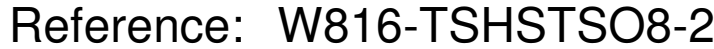
| Lot # | Diffusion Lot | Assy Lot | Trace Code | Process/ Package | Product Line | Comments |
|---|---|---|---|---|---|---|
| 1 | V66053FV | 9HL190060001 | G9714001 | SO8 | 0158 | |
| 2 | V66053FV | 9HL1900A0001 | G9714005 | SO8 | 0158 | |
| 3 | V66053FV | 9HL190090001 | G9714004 | SO8 | 0158 | |

Detailed results in below chapter will refer to P/N and Lot #.

## 6.2 Test plan and results summary

**P/N LM358DT**

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS | | | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Lot 1 | Lot 2 | Lot 3 | |
| **Die Oriented Tests** | | | | | | | | | |
| HTOL | N | JESD22 A-108 | Tj = 125°C, BIAS | 80 | 168 H | 0/80 | 0/80 | 0/80 | |
| | | | | | 500 H | 0/80 | 0/80 | 0/80 | |
| | | | | | 1000 H | 0/80 | 0/80 | 0/80 | |
| HTSL | N | JESD22 A-103 | Ta = 150°C | | 168 H | 0/77 | 0/77 | | |
| | | | | | 500 H | | | | |
| | | | | | 1000 H | 0/77 | 0/77 | | |
| ELFR | N | AEC Q100 - 008 | | 400 | 48H | 0/400 | 0/401 | 0/396 | |
| **Package Oriented Tests** | | | | | | | | | |
| PC | | JESD22 A-113 | Drying 24 H @ 125°C<br>Store 192 H @ Ta=30°C Rh=60%<br>Over Reflow @ Tpeak=260°C 3 times | | Final | PASS | PASS | PASS | |
| uHAST | Y | JESD22 A-118 | T°=130°C; Pressure=2.3 atm; HR=85% | | 96 H | 0/80 | 0/80 | | |
| THS | Y | JESD22 A-110 | Ta = 85°C, RH = 85%, | | 168 H | 0/80 | | | |
| | | | | | 1000 H | 0/80 | | | |
| TC | Y | JESD22 A-104 | Ta = -65°C to 150°C | | 100 cy | 0/77 | 0/77 | | |
| | | | | | 1000 cy | 0/77 | 0/77 | | |
| THB | Y | JESD22 A-101 | Ta = 85°C, RH = 85%, BIAS | | 168 H | 0/77 | 0/77 | 0/77 | |
| | | | | | 500 H | 0/77 | 0/77 | 0/77 | |
| | | | | | 1000 H | 0/77 | 0/77 | 0/77 | |
| **Other Tests** | | | | | | | | | |
| ESD | N | AEC Q101-001, 002 and 005 | CDM | 3 | 1.5kV | PASS | | | |


Reference: W816-TSHSTSO8-2

## Evaluation plan and preliminar results for P/N TS922IDT, L78L05ABD13TR, LD1117D33CTR

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS Lot 1 0922 | Lot 2 LA05 | Lot 3 KS33 | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | |
| HTB/ HTOL | N | JESD22 A-108 | Ta = 150°C, BIAS | | 168 H | 0/77 | 0/77 | 0/77 | | | |
| | | | | | 500 H | 0/77 | 0/77 | 0/77 | | | |
| | | | | | 1000 H | 0/77 | 0/77 | 0/77 | | | |
| HTSL | N | JESD22 A-103 | Ta = 150°C | | 168 H | 0/77 | 0/45 | 0/45 | | | |
| | | | | | 500 H | 0/77 | 0/45 | 0/45 | | | |
| | | | | | 1000 H | 0/77 | 0/45 | 0/45 | | | |
| | | | | | | | | | | | |
| **Package Oriented Tests** | | | | | | | | | | | |
| PC | | JESD22 A-113 | Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times | | Final | | | | | | |
| UHAST/ AC | Y | JESD22 A-102 | Pa=2Atm / Ta=121°C | | 96 H 168H | 0/77 | 0/77 | 0/77 | | | |
| TC | Y | JESD22 A-104 | Ta = -65°C to 150°C | | 100 cy | 0/77 | 0/77 | 0/77 | | | |
| | | | | | 200 cy | 0/77 | 0/77 | 0/77 | | | |
| | | | | | 500 cy | 0/77 | 0/77 | 0/77 | | | |
| | | | | | | | | | | | |
| THB | Y | JESD22 A-101 | Ta = 85°C, RH = 85%, BIAS | | 168 H | 0/77 | 0/77 | 0/77 | | | |
| | | | | | 500 H | 0/77 | 0/77 | 0/77 | | | |
| | | | | | 1000 H | 0/77 | 0/77 | 0/77 | | | |

# 7 ANNEXES

## 7.1 Device details

### 7.1.1 Package outline/Mechanical data

PACKAGE OUTLINE ASSEMBLY

TITLE: POA SO 8L

PLANT CODE: 999L
PACKAGE CODE: O7
PACKAGE WEIGHT: 0,0765 g/unit typ
JEDEC REFERENCE NUMBER: JEDEC MS-012-AA

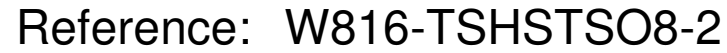
Option C

PACKAGE DIMENSIONS

| DATABOOK | | | | |
|---|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. | NOTE |
| A | - | - | 1.75 | |
| A1 | 0.10 | - | 0.225 | |
| A2 | 1.30 | 1.40 | 1.50 | |
| A3 | 0.60 | 0.65 | 0.70 | |
| b | 0.39 | - | 0.47 | |
| b1 | 0.38 | 0.41 | 0.44 | |
| c | 0.20 | - | 0.24 | |
| c1 | 0.19 | 0.20 | 0.21 | |
| D | 4.80 | 4.90 | 5.00 | |
| E | 5.80 | 6.00 | 6.20 | |
| E1 | 3.80 | 3.90 | 4.00 | |
| e | | 1.27BSC | | |
| L1 | | 1.05REF | | |
| h | 0.25 | - | 0.50 | |
| L | 0.50 | - | 0.80 | |
| Θ | 0 | - | 8° | |

NOTES:

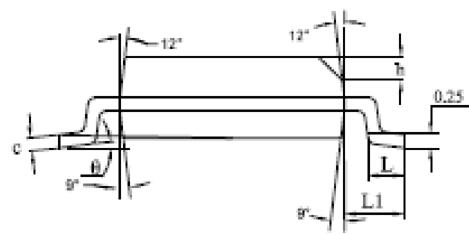
1. Controlling Dimension: MILLIMETER
2. Package outline exclusive of any mold flashes dimensions and metal burrs
3. Max resin gate protrusion : 0.20mm



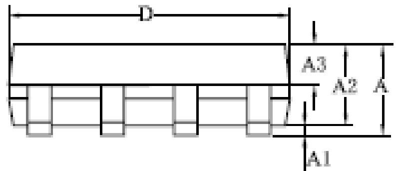

# PLANT CODE: 999L

## SO 8L

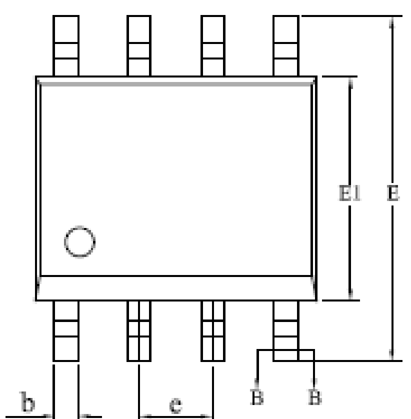
### SIDE VIEW

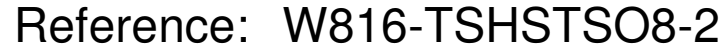



### SIDE VIEW



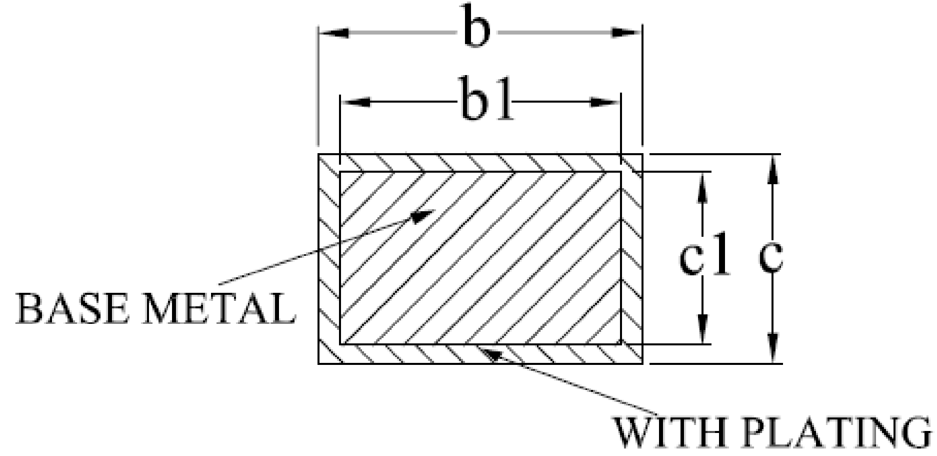

### TOP VIEW




Reference: W816-TSHSTSO8-2

# PLANT CODE: 999L

## SO 8L



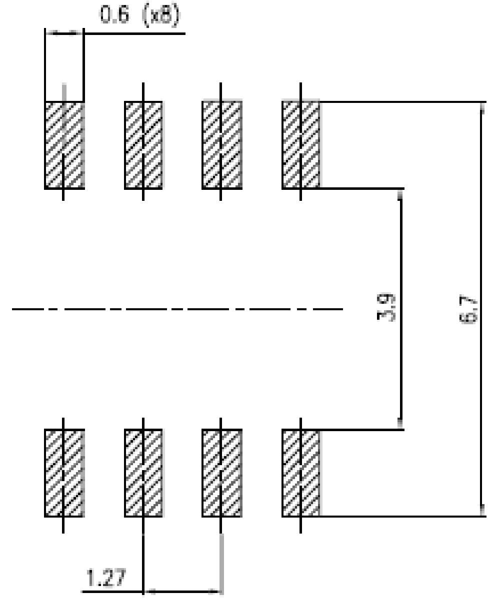

SECTION B-B

Reference: W816-TSHSTSO8-2

| FIGURE : 2 | DOC. NUMBER : 0016023 |
|---|---|

TITLE : PLASTIC SMALL OUTLINE PACKAGE 8L

# RECOMMENDED FOOTPRINT

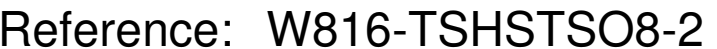



MATERIAL

NATIVE SCALE

PROJECTION

| DIM are in mm – Unspecified tolerance | | | | | | |
|---|---|---|---|---|---|---|
| Precision rate | 0 mm 6 mm | 6,01 mm 30 mm | 30,01mm 120 mm | 120,01mm 315 mm | over 315 mm | Angular |
| Coarse | ±0.2 | ±0.5 | ±0.8 | ±1.2 | ±2 | ±1° |
| Medium | ±0.1 | ±0.2 | ±0.3 | ±0.5 | ±0.8 | ±0°30' |
| Fine | ±0.05 | ±0.1 | ±0.15 | ±0.2 | ±0.3 | ±0°20' |



## 7.2 Tests Description

| Test name | Description | Purpose |
|---|---|---|
| **Die Oriented** | | |
| **HTOL**<br>Higt Temperature Operating Life<br><br>**HTB**<br>High Temperature Bias | The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition. | To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way.<br>The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults. |
| **HTSL**<br>High Temperature Storage Life | The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature. | To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding. |
| **ELFR**<br>Early Life Failure Rate | The device is stressed in biased conditions at the max junction temperature. | To evaluate the defects inducing failure in early life. |
| **Package Oriented** | | |
| **PC**<br>Preconditioning | The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption. | As stand-alone test: to investigate the moisture sensitivity level.<br>As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance.<br>The typical failure modes are "pop corn" effect and delamination. |
| **AC**<br>Auto Clave (Pressure Pot) | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature. | To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. |
| **TC**<br>Temperature Cycling | The device is submitted to cycled temperature excursions, between a hot and acold chamber in air atmosphere. | To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation. |
| **THB**<br>Temperature Humidity Bias | The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity. | To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence. |
| **Other** | | |
| **ESD**<br>Electro Static Discharge | The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models.<br>**CBM**: Charged Device Model<br>**HBM**: Human Body Model<br>**MM**: Machine Model | To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge. |

Annex 1: Other results

Wire pull test

| Value in gram (min limit 4g) | | | | | | |
|---|---|---|---|---|---|---|
| | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Unit 6 |
| | 23.67 | 23.97 | 22.2 | 21.1 | 22.17 | 20.99 |
| | 24.06 | 23.24 | 23.14 | 20.26 | 19.5 | 24.18 |
| | 19.33 | 24.01 | 21.18 | 23 | 25.42 | 19.36 |
| | 19.58 | 22.17 | 20.99 | 21.15 | 24.64 | 22.17 |
| | 20.16 | 20.35 | 24.87 | 22.87 | 24.2 | 20.5 |
| | 20.48 | 20.69 | 22.96 | 21.55 | 22.5 | 25.97 |
| | 20.77 | 21.29 | 21.34 | 21.51 | 21.3 | 24.64 |
| | 21.65 | 21.79 | 20.85 | 23.26 | 23.31 | 24.2 |
| Min(g) | 19.33 | | | | | |
| Max(g) | 25.97 | | | | | |
| average(g) | 22.09 | | | | | |
| cpl | 3.56 | | | | | |

Wire shear test

| Value in gram (min limit 18g) | | | | | | |
|---|---|---|---|---|---|---|
| | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Unit 6 |
| | 46.89 | 49.58 | 48.33 | 49.26 | 46.21 | 46.88 |
| | 48.15 | 46.33 | 46.27 | 47.55 | 48.71 | 49.54 |
| | 45.25 | 49.88 | 16.86 | 45.65 | 49.55 | 49.67 |
| | 48.22 | 48.37 | 48.17 | 48.14 | 46.35 | 49.18 |
| | 47.36 | 48.16 | 46.88 | 49.33 | 45.33 | 49.24 |
| | 48.31 | 48.87 | 47.33 | 48.98 | 49.36 | 48.98 |
| | 49.16 | 49.33 | 45.33 | 50.17 | 48.71 | 48.36 |
| | 48.24 | 47.24 | 46.24 | 48.98 | 49.36 | 48.78 |
| Min (g) | 16.86 | | | | | |
| Max (g) | 50.17 | | | | | |
| Average (g) | 46.67 | | | | | |
| cpl | 2.05 | | | | | |

Conclusion: in line with ST specification

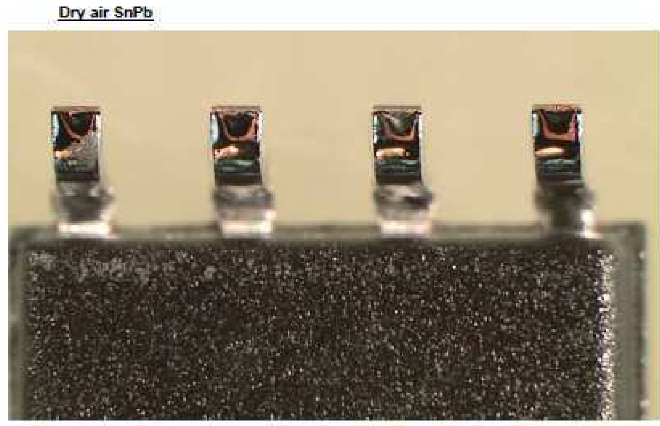
Solderability
Coverage minimum 95% after dipping

| PACKAGE | SOLDER BATH | SOLDER BATH TEMP. | SOLDER DIPPING TIME | AGING | SAMPLING | REJECT |
|---|---|---|---|---|---|---|
| **Lead finishing Sn Preplated** | SnPb | 220°C | 10s | 8h steam @85°C/85HR | 10 | 0 |
| | | | 10s | 16hrs dry air @150°C | 10 | 0 |
| | SnAgCu | 245°C | 10s | 8h steam @85°C/85HR | 10 | 0 |
| | | | 10s | 16hrs dry air @150°C | 10 | 0 |

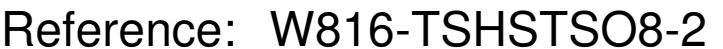
**Dry air SnAgCu**

**Steam SnPb**

**Dry air SnPb**



Conclusion: in line with ST specification.



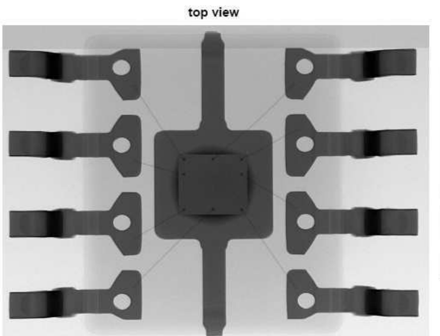

Electrical distribution compare to part produce in ST Bouskoura

| | | MEAN | | | CPK | |
|---|---|---|---|---|---|---|
| | **Units** | **TSHT** | **BSK** | **Mean Drift** | **TSHT** | **Comments** |
| **P106_*0** | **mA** | 0.45 | 0.46 | -0.01 | 50.38 | OK |
| **P101_A0** | **mV** | 0.26 | 0.49 | -0.23 | 3.03 | OK |
| **P101_B0** | **mV** | 0.98 | 1.26 | -0.27 | 3.07 | OK |
| **P117_A0** | **V** | 28.52 | 28.53 | -0.01 | 8.11 | OK |
| **P117_B0** | **V** | 28.53 | 28.52 | 0.01 | 8.55 | OK |
| **P117_A0** | **V** | 0.00 | 0.00 | 0.00 | 10.11 | OK |
| **P117_B0** | **V** | 0.00 | 0.00 | 0.00 | 9.14 | OK |
| **P106_*1** | **mA** | 0.56 | 0.62 | -0.05 | 30.83 | OK |
| **P101_A1** | **mV** | 0.25 | 0.46 | -0.21 | 2.82 | OK |
| **P101_B1** | **mV** | 1.00 | 1.23 | -0.23 | 2.38 | OK |
| **P106_*3** | **mA** | 0.47 | 0.50 | -0.03 | 13.11 | OK |
| **P101_A3** | **mV** | 0.24 | 0.47 | -0.23 | 2.86 | OK |
| **P101_B3** | **mV** | 0.98 | 1.23 | -0.25 | 2.43 | OK |
| **P101_A2** | **mV** | -0.03 | 0.23 | -0.26 | 2.97 | OK |
| **P101_B2** | **mV** | 0.68 | 0.99 | -0.31 | 2.66 | OK |
| **P105_A1** | **dB** | 128.55 | 129.38 | -0.83 | n/a . | OK |
| **P105_B1** | **dB** | 119.44 | 133.49 | -14.05 | n/a . | OK |
| **P109_A1** | **dB** | 100.65 | 102.89 | -2.24 | n/a . | OK |
| **P109_B1** | **dB** | 99.57 | 102.83 | -3.26 | n/a . | OK |
| **P104_A1** | **V/mV** | 302.14 | 253.98 | 48.15 | n/a . | OK |
| **P104_B1** | **V/mV** | 318.47 | 259.78 | 58.69 | n/a . | OK |
| **P115_*1** | **n/a** | 1.00 | 1.00 | 0.00 | n/a . | OK |
| **P150_*1** | **V** | 5.00 | 5.00 | 0.00 | 3024.28 | OK |
| **P117_A3** | **mV** | 0.00 | 0.00 | 0.00 | 8.43 | OK |
| **P117_B3** | **mV** | 0.00 | 0.00 | 0.00 | 8.29 | OK |
| **P117_A1** | **V** | 28.20 | 28.45 | -0.24 | 70.80 | OK |
| **P117_B1** | **V** | 28.21 | 28.44 | -0.23 | 69.45 | OK |
| **P117_A5** | **V** | 8.52 | 8.53 | -0.01 | 14.79 | OK |
| **P117_B5** | **V** | 8.53 | 8.53 | -0.01 | 14.46 | OK |
| **P117_A3** | **V** | 3.62 | 3.59 | 0.03 | 8.21 | OK |
| **P117_B3** | **V** | 3.62 | 3.59 | 0.03 | 8.13 | OK |
| **P101_A31** | **mV** | 0.00 | 0.00 | 0.00 | 3.19 | OK |
| **P101_B31** | **mV** | 0.00 | 0.00 | 0.00 | 3.28 | OK |
| **P102_A1** | **nA** | -1.85 | 0.00 | -1.85 | n/a . | OK |
| **P102_B1** | **nA** | -3.92 | 0.00 | -3.92 | n/a . | OK |
| **P103_A1** | **µA** | -0.0395 | -0.0311 | -0.0084 | n/a . | OK |
| **P103_B1** | **µA** | -0.0403 | -0.0324 | -0.0079 | n/a . | OK |
| **P103_A1** | **µA** | -0.0377 | -0.0306 | -0.0071 | n/a . | OK |
| **P103_B1** | **µA** | -0.0364 | -0.0298 | -0.0066 | n/a . | OK |
| **P137_A2** | **mA** | 0.0180729 | 0.0183346 | -0.0002617 | 20.07 | OK |
| **P137_B2** | **mA** | 0.0182641 | 0.0184874 | -0.0002233 | 18.19 | OK |
| **P137_A1** | **mA** | -0.03 | -0.03 | 0.00 | 18.23 | OK |
| **P137_B1** | **mA** | -0.03 | -0.03 | 0.00 | 20.08 | OK |
| **P137_A21** | **mA** | 0.08 | 0.00 | 0.08 | 13.39 | OK |
| **P137_B21** | **mA** | 0.08 | 0.00 | 0.08 | 10.34 | OK |
| **P121_A1** | **MHz** | 1.19 | 1.27 | -0.08 | 13.47 | OK |
| **P121_B1** | **MHz** | 1.22 | 1.27 | -0.05 | 13.07 | OK |
| **P113_A2** | **V/uS** | 0.84 | 0.82 | 0.02 | 20.08 | OK |
| **P113_B2** | **V/uS** | 0.85 | 0.86 | -0.01 | 19.50 | OK |
| **P113_A2** | **V/uS** | 0.73 | 0.71 | 0.02 | 15.39 | OK |
| **P113_B2** | **V/uS** | 0.73 | 0.74 | -0.01 | 20.00 | OK |

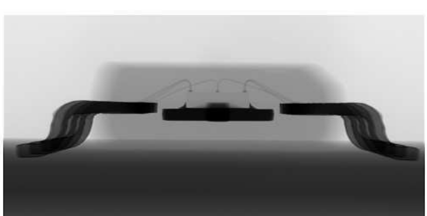
**No CPK calculation done on the Iib, AVD, CMR, SVR as they are not gaussian**

Xray pictures

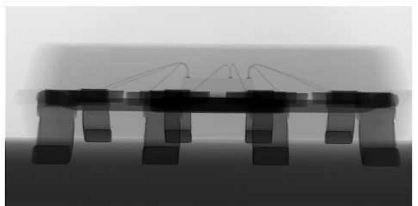
top view



side 1 view 45°



side 2 view 45°



Process flow chart:

| 序号 NO. | 工艺流程 PROCESS FLOW | 工艺步骤 PROCESS STEP |
|---|---|---|
| | | 晶圆&芯片 Wafer & Chip |
| | | 反馈客户 Feedback Customer |
| 1 | Pass / Fail | 晶圆进料检验 Wafer IQC |
| 2 | BG TAPE | 晶圆正面贴膜（可选） BG Tape(Option) |
| 3 | Back Grinding | 减薄 Back Grinding |
| 4 | Wafer Mounting | 贴片 Wafer Mounting |
| 5 | WFT_BK | 贴片预烘烤Wafer Mounted Tape rebake |
| 6 | Wafer Sawing | 划片 Wafer Sawing |
| | | 引线框架 Lead frame |
| | | 贴片材料 Die Attach Material |
| 7 | Die Bonding | 上芯 Die Bonding |
| 8 | DA Curing | 上芯烘烤 DA Curing |

| 序号 NO. | 工艺流程 PROCESS FLOW | 工艺步骤 PROCESS STEP |
|---|---|---|
| 9 | Plasma before W/B | 压焊前清洗 Plasma before Wire bond |
| | | 焊线 Bonding Wire |
| 10 | Wire bonding | 压焊 Wire Bonding |
| 11 | | 品管检验 QC Gate |
| | | 塑封料 Mold Compound |
| 12 | Molding | 塑封 Molding |
| 13 | PMC | 后固化 Post Mold Curing |
| | | 锡球 Pin Sn |
| 14 | Plating | 电镀 Plating |
| 15 | Cure after Plating | 电镀后烘烤 Cure after Plating |
| 16 | Laser Marking | 激光打印 Laser Marking |

| 序号 NO. | 工艺流程 PROCESS FLOW | 工艺步骤 PROCESS STEP |
|---|---|---|
| 17 | Trim/Form/ Singulation | 切筋/成形/分离 Trim/Form/Singulation |
| 18 | | 品管检验 QC Gate |
| 19 | FT | 测试（可选） Testing(Option) |
| 20 | | EQC品管检验（可选） EQC Gate (Option) |
| 21 | | VI 品管检验（可选） Visual Inspection Gate(Option) |
| 22 | Packing | 包装 Packing |
| 23 | | 品管检验 Outgoing quality control |
| 24 | Shipping | 发货 Shipping |

## 7.3 Product list

| Commercial products from Shenzhen |
|---|
| LM2931AD50R |
| LM2931D-R |
| LM2931AD33R |
| LD1117D33CTR |
| LD1117D33TR |
| L78L05ABD13TR |
| L78L05ACD13TR |
| L78L05CD13TR |
| L78L06ACD13TR |
| L78L08ABD13TR |
| L78L08ACD13TR |
| L78L08CD13TR |
| L78L09ABD13TR |
| L78L09ACD13TR |
| L78L09CD13TR |
| L78L12ABD-TR |
| L78L12ACD13TR |
| L78L12CD13TR |
| L78L15ACD13TR |
| L78L15CD-TR |
| LM217LD13TR |
| LM317LD13TR |
| L78L18CD13TR |
| L78L24CD-TR |
| L78L33ABD-TR |
| L78L33ACD13TR |
| L78L33CD-TR |
| L79L05ABD13TR |
| L79L05ACD13TR |
| L79L08ACD13TR |
| L79L12ACD13TR |
| L79L15ABD13TR |
| L79L15ACD13TR |
| LE30CD-TR |
| LE50ABD-TR |
| LE50CD-TR |
| LE80CD-TR |
| LE33CD-TR |
| LE45CD-TR |

Reference:  W816-TSHSTSO8-2

| **Commercial products  from Bouskoura** |
| --- |
| LF253DT |
| LF351D |
| LF351DT |
| LF353DT |
| LM833DT |
| MC4558CDT |
| MC4558IDT |
| TJM4558CDT |
| TL061CDT |
| TL062CD |
| TL062CDT |
| TL071CDT |
| TL072CD |
| TL072CDT |
| TL081CDT |
| TL082CD |
| TL082CDT |
| TS922ID |
| TS922IDT |
| TS952IDT |